Corporate Overview

February 2003

Virtual Silicon

A leading supplier of semiconductor intellectual property to SoC designers and manufacturers.

Virtual Silicon

- Founded 1997 in Sunnyvale, California
- Seasoned Management Team of IP Pioneers
- $42M of Financial Backing Through Series C
- Established Tier 1 Customers
  - Infineon, Agilent, AMD
- Broad Network of EDA & IP Partners
- Worldwide Sales and Distribution Channels
- 62 Full-time Employees in Silicon Valley

Positive Momentum:
Technology, Customers, Revenue Growth

Management Team

Executive Officers

Barry Hoberman
CEO and President

Howard Hideshima
Vice President of Finance and CFO

Bill Becker
Vice President, Engineering

John Ford
Vice President, Marketing and European Sales

Fern Forcier
Vice President of Program Management

Dan Hillman
Vice President of Business Operations & Infrastructure

Mahesh Tirupattur
Vice President of Pacific Rim and North American Sales

Board of Directors

Barry Hoberman
CEO and President

Michael Kliment
Founder

Bernie Aronson
President, Synplicity

Daniel Faizullabhoy
General Partner, Walden International

Sam Lee
Managing Director, Infinity Capital LLC

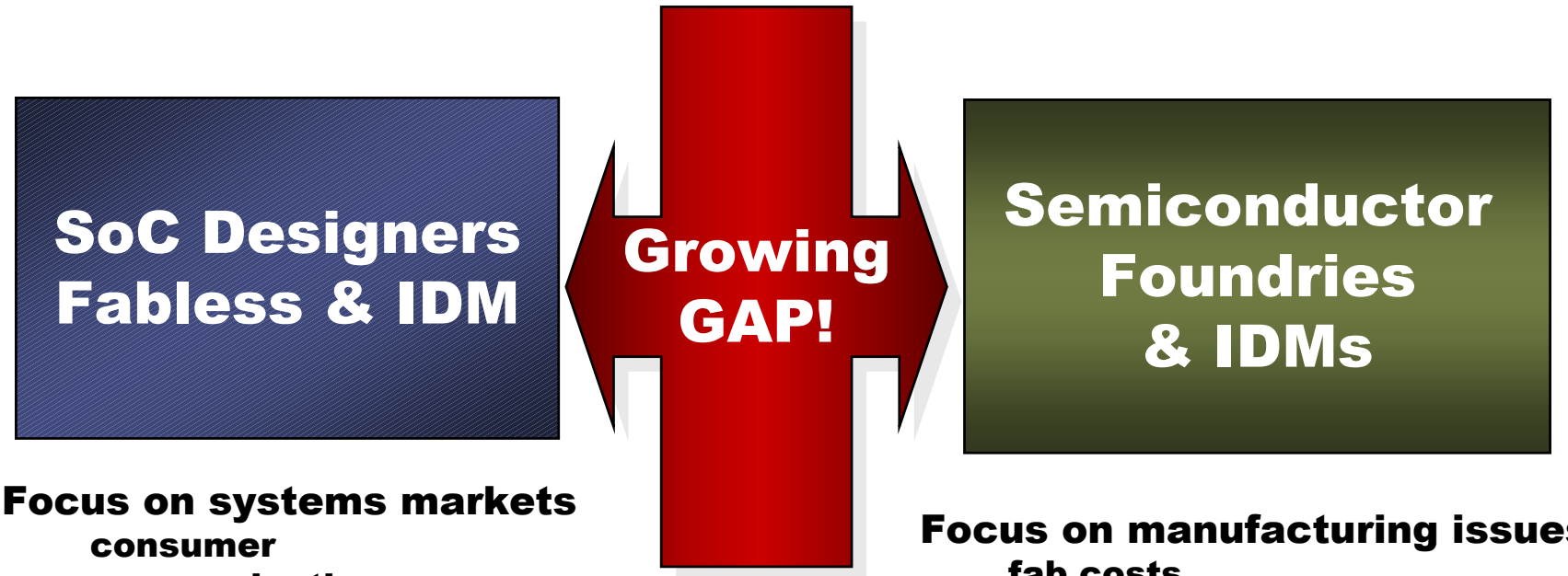
Douglas Lindgren
Managing Director, US Trust Private Equity

Strategy

- To be the Primary Source of Process Specific Semiconductor IP to SoC Designers and Manufacturers
  - **By providing best in class SoC IP including standard cell libraries, I/O, and embedded SRAM and ROM memory solutions**
  - **By providing high-value, process-intensive IP blocks including high-speed interface, PLLs, connectivity solutions**

Best in Class Total IP Solution

Growing Specialization



Focus on systems markets
- consumer
- communications
- computing

Focus on design complexity

Systems-on-chip solutions

Loss of manufacturing expertise

Focus on manufacturing issues
- fab costs
- capacity planning

Focus on process technology

Loss of systems design expertise

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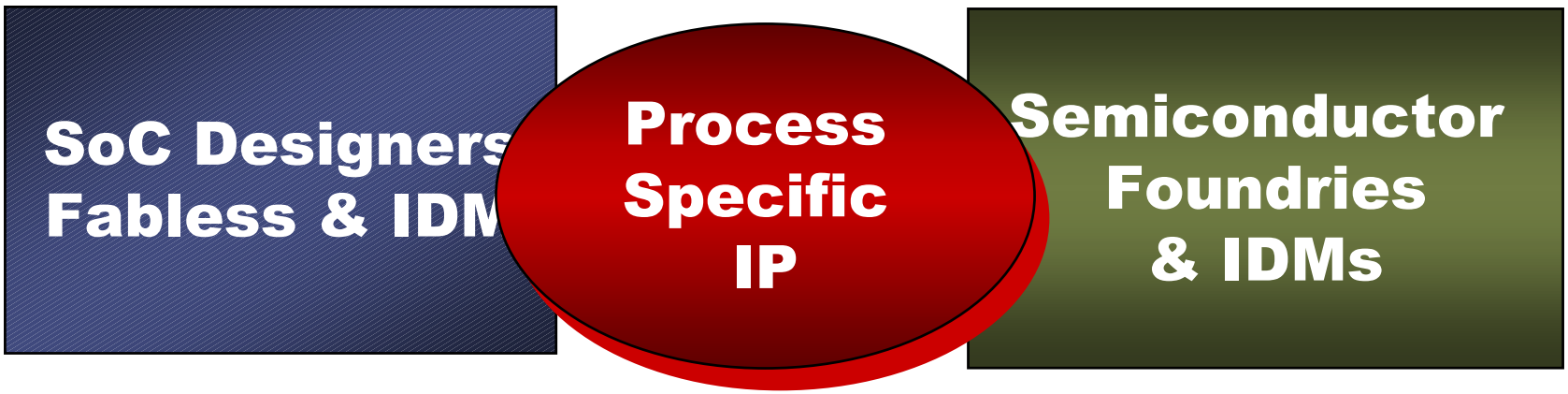
IP - The Critical Link



Infrastructure For SoC Designers and Fabs

Virtual Silicon

Core Competencies

Competence	Customer Benefit
Process Expertise	1st- to - Market
Silicon Ready®	Verified IP
Broad Offering	Reduce # of Vendors IP Compatibility
Process Automation	Faster, More Accurate Technology Ports
Foundry Endorsement	Reduce Risk

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Growing Foundry Portfolio

	1st Silicon	IBM	TSMC	UMC
Standard Cells	Yes	Yes		Yes
Memory	Yes		Yes	Yes
I/Os & Interface	Yes	Yes	Yes	Yes
PLL	Yes	Yes	Yes	Yes

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Growing Technology Portfolio

	0.25µ	0.18µ	0.15µ	0.13µ	90 nm
Standard Cells	Yes	Yes	Yes	Yes	Dev.
SRAM, ROM & MPRF	Yes	Yes	Yes	Yes	Dev.
I/Os & Interface	Yes	Yes	Yes	Yes	Dev.
PLL	Yes	Yes	Yes	Yes	Dev.

Virtual Silicon

Partners

- **Foundries**
  - 1st Silicon, Hynix, IBM, TSMC & UMC
- **EDA Vendors**
  - Cadence, Genesys Testware, Logic Vision, Magma, Mentor, Numerical Technologies, Silicon Metrics, Synopsys, Verplex
- **Design Service Partners**
  - Cadence Design Foundry, eSilicon, IMEC/Europractice, Nordic VLSI, Synopsys Professional Services

Top 20 Ranked Customers

IDM[1]

- **Intel**
- Toshiba
- STM
- TI
- Samsung
- **NEC**
- **Hitachi**
- Motorola
- **Infineon**
- Philips
- IBM
- **AMD**
- Mitsubishi
- Matsushita
- Fujitsu
- Agere
- Sanyo
- **Hynix**
- Micron
- **Sony**

ASIC[1]

- IBM
- Agere
- **LSI Logic**
- **NEC**
- **Xilinx**
- Fujitsu
- Altera
- Toshiba
- Mitsubishi
- **Agilent**
- STM
- Philips
- **Atmel**
- **Alcatel**
- Lattice
- TI
- Samsung
- Sharp
- **Hitachi**
- AMI

Fabless[2]

- Qualcomm
- Nvidia
- **Xilinx**
- **Broadcom**
- Altera
- **Cirrus Logic**
- **Adaptec**
- SanDisk
- QLogic
- PMC-Sierra
- **Lattice**
- SST
- **Terayon**
- ESS
- Globespan
- **Centillium**
- SMC
- ICS
- **Actel**
- Oak Tech

Foundry[1]

- **TSMC**
- **UMC**
- Other
- **Chartered**
- AMI
- **IBM**
- Fujitsu
- **Hynix**
- Agere
- Tower
- Samsung
- **1st Silicon**

[1]**Dataquest 2001**

[2]**FSA 2001**

Red = Virtual Silicon Customers/Partners

Virtual Silicon

Broad Choice of EDA Tools

	Cadence	Mentor	Synopsys
Synthesis	PKS/Build Gates		Design Compiler & Physical Compiler, Power Compiler
Simulation	NCsim	ModelSim	VCS
Timing & Power	Pearl/TLF		PrimeTime PrimePower
Physical Design	Silicon Ensemble		Apollo Astro
Extraction and Delay Calc.			Arcadia
DRC/LVS	Assura	Calibre	
Testability		Fastscan, DFT	DFT, TetraMax

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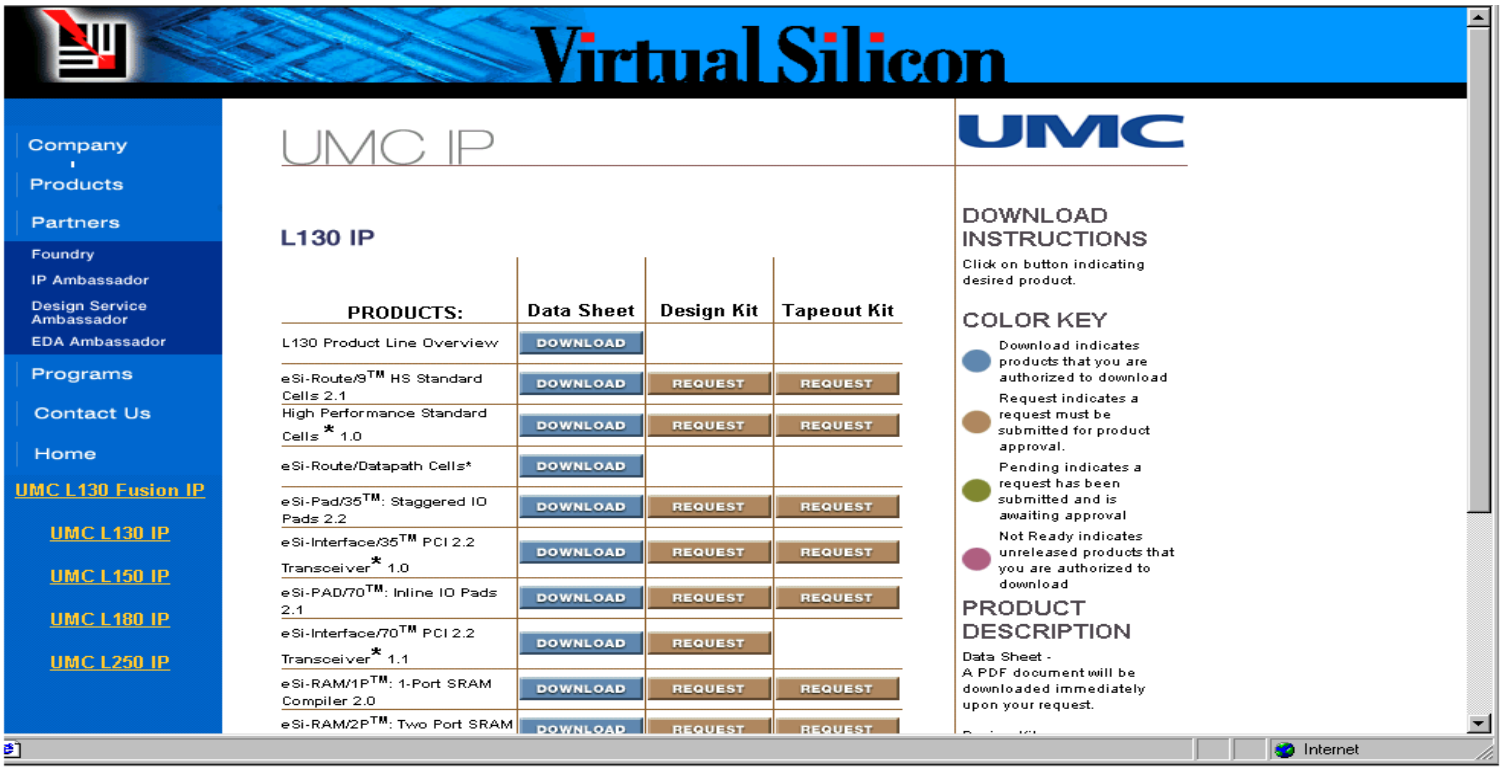
IP Internet Download



Virtual Silicon

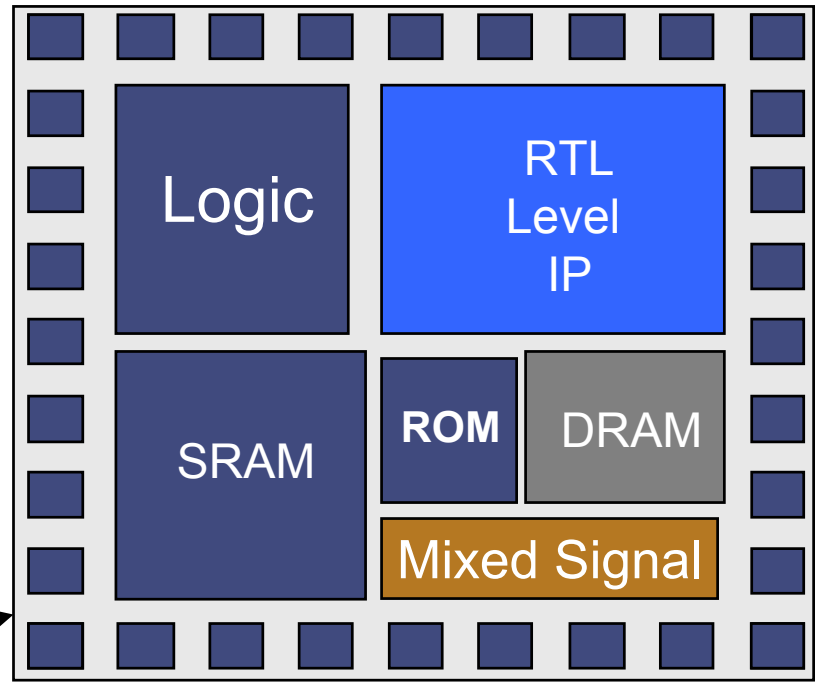
Products

Basic I/O Pads
High Speed Connectivity Solutions
PLL and PLL Compilers
Standard Cell Libraries
SRAM & ROM Compilers & Instances
Multi Port Register Files Instances

Multiple Foundry Solutions; UMC, TSMC, IBM & Others

Integrated Portfolio of SOC IP

- Process-specific IP for nearly every component of advanced SoCs
- Offering covers 85% of all SoC applications
- Serves more than any other IP vendor



Virtual Silicon IP
Built with Virtual Silicon IP
Roadmap
Not Served

Virtual Silicon

Standard Cells

- Highest Density Standard Cells
  - Hand-crafted layouts that use only metal 1 layer inside cells
  - Multiple pickups and high porosity for highest router utilization
- Widest Choice of Application Specific Cell Sets
  - High performance for graphics & communications
  - Low power for portable & consumer markets
- Most Accurate Characterization for Leading Design Tools
  - Timing data for synthesis, simulation and static timing analysis
  - Power data for optimized construction and power analysis

RAM and ROM

- High performance synchronous SRAMs
  - Small cell size and handcrafted layout for optimized block size
  - Low standby and leakage current
  - Single-port, dual-port and two port
- High performance Multi-port register files for data buffering
  - Offered in instance or compiler form
  - Web based front end instance generator
  - Synchronous and Asynchronous
- Diffusion and metal-programmable ROMs
  - Synchronous and asynchronous
  - High density of up to 1Mb for the diffusion ROM

I/O & Interface

- Pads - Over 200 Standard CMOS/TTL I/O Functions
  - 3.3V capable and 5VT I/Os with built-in level shifters
  - Both staggered and in-line architectures supported
  - Specialty I/O for analog signals and power domains
  - Crystal Oscillators Pads
- Interface - Application Specific I/O Functions
  - DDR & QDR Solution; SSTL-2, HSTL I & II
  - LVDS 622 MHz./1.25 GHz.
  - PCI 2.2, PCI-X, USB 1.1 & AGP4X

PLL Compilers

- PLL generator for high performance applications
  - Clock de-skew, frequency multiplication, jitter removal
- High precision, low jitter, silicon proven accuracy
- User selected center and output frequencies
- Fully automated EDA model and layout generation
- Compiler can be ported to any standard process

PLL Instances

- Custom PLL for higher performance and specialty applications
- Super high frequencies
- Multiple phase clock generation
- Programmable frequency multiplication
- High precision frequency synthesizers
- Programmable clock phase delays
- Clock Data Recovery circuits
  - Infiniband, Rapid I/O, Hypertransport and Custom interfaces

UMC Sponsored IP

- UMC has Paid Virtual Silicon to Develop Basic IP Components for L250, L180, L150 & L130 Processes
- Virtual Silicon Distributes this IP at No Charge to UMC Customers via Internet Download System
- Basic Support is Included in this Program
- Complete Solutions for SoC Designs

1st Silicon Sponsored IP

- 1st Silicon has Paid Virtual Silicon to Develop Basic IP Components for 0.18 µm Process
  - Standard Cells
  - Clock Gating Standard Cells
  - In-line Basic I/O
  - Staggered Basic I/O
  - 1P SRAM Compiler
- Virtual Silicon Distributes this IP at No Charge to 1st Silicon Customers via Internet Download System

Application Engineering Support

- Basic Maintenance is Targeted to Satisfy Sophisticated COT Designers with Internal Capability for
  - Test Chip
  - EDA Flows
  - Product Engineering
  - Test Engineering
- Support Packages are Available for Customers Who Want
  - Non Standard EDA Flows
  - Early Access to New Products
  - Access to Development Eng'g and Program Management

Customer Testimonials

Our SoC designers need to get the last ounce of performance from our silicon to achieve our performance goals and still meet our aggressive product delivery schedules. Virtual Silicon's IP gave us that extra advantage to allow us to achieve our performance and schedule goals."

John Szetela, Manager of CAD Systems Eng'g

AMD

"We have used their IP in our leading FPGA products with great success. Virtual Silicon has developed innovative IP architectures for advanced silicon processes and has provided accurate EDA views."

Steve Douglass, Director of Product Development

Xilinx

"We chose Virtual Silicon because of their track record in delivering reliable, high performance libraries to meet our aggressive market windows. Virtual Silicon was there for us where it counts."

Greg Buchner, Vice President, Engineering

ATI Technologies, Inc.

Virtual Silicon

Why Virtual Silicon?

- Comprehensive Process Specific SoC IP Solution
- Best In Class Silicon Expertise
- Best In Class Silicon Verification
- Innovative Product Technology
- Virtual Silicon has Earned the Reputation as...

Your Source for IP

Virtual Silicon